bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ■ V1.01
Firmware for BDI3000 ■ V1.06

Date: April 10, 2008

Error Correction

• Cortex-A8: Correct fast/stalled memory access sequences.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.01
Firmware for BDI3000 ■ V1.07

Date: July 9, 2008

Enhancements

- Support for ARM1176 and Cortex-M3 (STM32) added.
- Support for STM32F10xx internal flash programming added.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.01
Firmware for BDI3000 ■ V1.08

Date: Aug. 29, 2008

Enhancements

- Support for Luminary Micro Stellaris LM3S internal flash programming added.
- Support for Cortex-M3 / Cortex-A8 Single Wire Debug Mode added (different firmware).

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ■ V1.02
Firmware for BDI3000 ■ V1.09

Date: Febr. 25, 2009

Enhancements

- Support for Cortex-R4 added
- Support for ARM7 connected via JTAG-AP added (see manual).
- New parameter to select the single step mode added (see manual).
- New Telnet commands INTENA and INTDIS added.

Error Correction

- Correct single step of newer ARMv6/v7 instructions.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.02
Firmware for BDI3000 ■ V1.10

Date: Sept. 29, 2009

Enhancements

- Support for DAP-Lite module added.
- Support for multiple A8/A9 debug components behind one DAP added.
- Support for searching nested ROM tables added.
- APB base address of the debug component can be preset (no ROM table search).
- Download speed via GDB improved.
- Support for a different reset type for the initial power-up reset added (see manual).

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.02
Firmware for BDI3000 ■ V1.11

Date: May 17, 2010

Enhancements

- Support for Atmel SAM3U / SAM3S internal flash programming added.
- SWD: Single Wire Output can be routed to a TCP/IP channel (see manual).

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.02
Firmware for BDI3000 ■ V1.12

Date: August 20, 2010

Enhancements

- Support for Cortex-M0 added.
- Support for LPC1xxx flash programming added.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ■ V1.03
Firmware for BDI3000 ■ V1.13

Date: Dec. 23, 2010

Enhancements

- Support for STM32L15 internal flash programming added.
- Support for EFM32 internal flash programming added.
- A8: Correct handling of synchronous watchpoints (step over during a restart).
- Get actual number of implemented break/watch points from DIDR register.

Error Correction

- M3: Correct sequence to set debug control bits (e.g. C_MASKINTS) before resume.
- A8/R4: Correct sequence to set PC before resume (use mov pc,r0 instead of bx r0).

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.03
Firmware for BDI3000 ■ V1.14

Date: April 1, 2011

Enhancements

- Support for Cortex-M4 added.
- Support for Freescale Kinetis internal flash programming added.
- New EXEC init list entry added (see manual).
- Special DAPPC configuration parameter added for TI processors (see manual).
- New Telnet MMU command allows to disable / enable the MMU.
- New PMM (Physical Memory Mapped) register type accesses memory always with disabled MMU.
- The BDI no longer automatically steps over a GDB set breakpoint at the current PC. This allows to use the GDB „jump“ command.

Error Correction

- A8/R4: Correct setting of instruction HWBP (Byte Select in BCR) for Thumb / Big Endian code.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.03
Firmware for BDI3000 ■ V1.15

Date: November 29, 2011

Enhancements

• Support for STM32F2 and STM32F4 internal flash programming added.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ■ V1.05
Firmware for BDI3000 ■ V1.16

Date: June 22, 2012

Enhancements

- New startup mode „idle“ added. An idle core will not be accesses until attached via Telnet.
- New Telnet command „state“ shows the state of all cores.
- New Telnet commands „attach“ and „detach“ added.
- New SCANINIT command „m“ allows to write to AHB memory space.
- Windows setup tool works now also with COM ports >= 10.
- Windows setup tool accepts the config file name as command line parameter.
- Support for Spansion S29VS-R flash added (S29VSRX16 algorithm)
- The JTAG clock frequency can be entered in Hertz and not only as an index.
- GDB: The BDI now answers with 1 to the GDB qAttached packet.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.05
Firmware for BDI3000 ■ V1.17

Date: April 2, 2013

Enhancements

- Support for STM32W internal flash added.
- Support for STM32F10 dual bank flash (XL-density) added.
- Maximal Telnet and GDB remote command length increased to 256 characters.
- Telnet command UPDATE added that allows to reload the configuration file without booting the BDI.
- The reset pin is no longer observed when reset mode NONE is defined.
- The Telnet commands attach and detach accept a core number as parameter.
- Kinetis: FSEC is programmed to unsecure also after a chip erase.
- Kinetis: Programming FSEC to a secure state is refused.
- Kinetis: Info about how to unsecure a secured device added (see kinetis_unsecure.cfg).
- Accept APB debug base addresses below 0x80000000 in order to support BCM5301x.
- Telnet access to FP registers for Cortex-A and Cortex-R added (rdfp and rmfp command).
- Support for Cortex-A5, Cortex-A7 and Cortex-A15 added.
- Cortex-A: Clear OS Lock Access bit after target power-up.
- Support for Cortex-M external flash programming with workspace added (Thumb algorithm). Output an error for not supported Flash/Buswidth combinations instead of simply loading the ARM algorithm.
- Support for simple bit manipulation (read/modify/write) via init list added. The RMx entry defines the address, the size and an optional XOR pattern.

```
RM8  <address> [<xor<]
RM16 <address> [<xor<]
RM32 <address> [<xor<]
WMX  <and> <or>
Example:
   RM32 0x20000000 0x10101010  ;read and XOR
   WMX  0xff00ff00 0x00000003  ;AND, OR and write back
```

- Init list entry added that waits until memory becomes a defined value. The RMx entry defines the address and the size for the following WAIT.

```
RM8  <address>
RM16 <address>
RM32 <address>
WAIT <mask> <equal>
Example:
   RM16 0x2000000a             ;define address and size
   WAIT 0x0000f0ff 0x00001034  ;wait until ((value & mask) == equal)
```

bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.05
Firmware for BDI3000 ■ V1.18

Date: August 9, 2013

Enhancements

- Support for STM32F0 internal flash added.
- Support for Kintetis FTFE and FTFA internal flash added.
- The WREG init list entry now accepts all names from the register definition file.
- Telnet access to 64-bit CPxx registers added (see user‘s manual).
- New Telnet command MODE allows to switch current processor mode.
- Cortex-A: New Telnet commands SECURE and NONSECURE allows to switch secure state.
- Cortex-M: AHB access port select parameter added. Used for Vybrid Cortex-M4 debug accesses.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ■ V1.06
Firmware for BDI3000 ■ V1.19

Date: March 5, 2014

Enhancements

- Support for ARM BE8 big endian mode added.
- Cortex-A: Improved core halted detection.
- Cortex-A: A new configuration parameter enables CTI support and defines the APB base address of the CTI component. It also defines the core group used when GDB sends the "continue" command.
- New and changed Multi-Core related Telnet commands.
- Configuration and register definitions can be stored in the BDI internal Flash memory. In this case no TFTP server is necessary to load the configuration files.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.06
Firmware for BDI3000 ■ V1.20

Date: May 30, 2014

Enhancements

• The BREAKMODE configuration parameter allows to set the break/watch control bits SSC, HMC and PMC in DBGBCR and DBGWCR:

BREAKMODE {SOFT | HARD} [{HYP | <control>}]
HYP adds the hypervisor mode bit to the control value
<control> defines the SSC, HMC and PMC bits in DBGBCR and DBGWCR
Default is SSC=00, HMC=0 and PMC=11 (0x00000006)

Examples:

```
BREAKMODE SOFT                ;control = 0x00000006
BREAKMODE HARD                ;control = 0x00000006
BREAKMODE HARD HYP            ;control = 0x00002006
BREAKMODE HARD 0x00002006     ;control = 0x00002006
```

• New Telnet QUERY command to display parts of the configuration.

QUERY [<core>]
Examples:

```
BDI> query      displays common and core specific configuration for all cores
BDI> query 1    displays the core specific configuration of the selected core
```

Error Correction

• The CTI registers of not attached cores are no longer accessed during multi-core restart.

bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.06
Firmware for BDI3000 ■ V1.21

Date: Nov. 4, 2014

Enhancements

- Support for Freescale LS1 (ARMv7, LS1021A, ...) added.
- SWAP option for register definitions added. Useful when accessing big endian registers from a little endian core or vice versa.
- A new configuration parameter option allows to define the protection bits for AHB/AXI accesses.
- For LS1, memory accesses via System Access Port (SAP) are supported.
- Maximal number of cores increased to 16.

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bdiGDB for BDI3000 ARM11 / Cortex

Release Note

Config. program ☐ V1.06
Firmware for BDI3000 ■ V1.22

Date: July 3, 2015

Enhancements

- Core halted detection: Check only HALT bit in DSCR, ignore Monitor Debug Mode.
- Process init list entries for running cores if possible (memory access AHB/SAP).

Error Correction

- Cortex-R4: Correct handling of instruction big endian mode.
- Display correct STEPMODE in Telnet QUERY command.
- Display correct CPUTYPE in Telnet QUERY command for LS1000.
- Correct handling of core numbers > 9 (#nbr) in the configuration file.

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