Addendum

DSP56303UMAD/D
Rev. 0, 05/2002

DSP56303 User's Manual Addendum

MOTOROLA intelligence everywhere™ | digital dna™

CONTENTS

1 Introduction

This document provides updated information for revision 1 of the *DSP56303 User's Manual (DSP56303UM/D)*. The updates include the following:

- Modified signal definitions
- New Operating Mode Register (OMR) layout and bit definitions
- New Bus Control Register (BCR) layout and bit definitions
- Updated SCI Receive Register (SRX) Description
- Updated Programming sheets for the OMR, BCR, and Address Attribute Registers (AAR[3–0])

2 Modified Signal Definitions

Area to Change	Change Description
Table 2-1, p. 2-1	• For Notes 1–4, delete the last sentence in each note. All internal keepers are disabled and do not affect device operation. • Change Ground (GND) to Ground (GND)[5]. • Change Note 5 to read as follows: **5**. The number of Ground signals listed are for the 144-pin TQFP package. For the 196-ball MAP-BGA package, there are 66 GND connections.
Figure 2-1, p. 2-2	• In the figure, change **Grounds:** to **Grounds[4]:** • At the bottom of the figure, add the following: **4**. The GND signals are listed for the 144-pin TQFP package. For the 196-ball MAP-BGA package, all grounds except GND_P and GND_{P1} are connected together and referenced as GND. There are 64 GND connections.
Table 2-3, p. 2-4	• Change the note at the end of the table to the following: **Note:** The subsystem GND signals (GND_Q, GND_A, GND_D, GND_C, GND_H, and GND_S) are listed for the 144-pin TQFP package. For the 196-ball MAP-BGA package, all grounds except GND_P and GND_{P1} are connected together inside the package and referenced as GND.
Table 2-8, pp. 2-7 to 2-8	• Change $\overline{BR}$ signal **State During Reset, Stop, or Wait** to: Reset: Output (deasserted) State during Stop/Wait depends on BRH bit setting: • BRH = 0: Output, deasserted • BRH = 1: Maintains last state (that is, if asserted, remains asserted) • Change $\overline{BB}$ signal State During Reset, Stop, or Wait to Ignored input

Area to Change	Change Description
Table 2-11, pp. 2-11 to 2-14	• Change the title of the third column to **State During Reset**[1,2]. • Add note 1 that states: **Note: 1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated. • Change the old note 1 to note 2. • Change **State During Reset** for all signals to Ignored input. • Change the signal description for PB14 to: **Port B14**—When the HI08 is configured as GPIO through the HPCR, this signal is individually programmed through the HDDR.
Table 2-12, pp. 2-15 to 2-16 **Table 2-13**, pp. 2-17 to 2-18 **Table 2-14**, p. 2-19 **Table 2-15**, p. 2-20	• Delete the **Stop** column • Change the title for the third column to **State During Reset** [1,2] Change **State During Reset** for all signals to Ignored input. **Note: 1.** In the Stop state, the signal maintains the last state as follows: • If the last state is input, the signal is an ignored input. • If the last state is output, these lines are tri-stated. • Change the old note 1 to note 2.

3 Operating Mode Register (OMR) Layout and Definition

Area to Change	Change Description
Figure 4-2, p. 4-15	Replace with the following:

Stack Control/Status (SCS)								Extended Operating Mode (EOM)								Chip Operating Mode (COM)							
23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
			SEN	WRP	EOV	EUN	XYS	ATE	APD	ABE	BRT	TAS	BE	CDP[1–0]		MS	SD		EBD	MD	MC	MB	MA
Reset:																							
0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	*	*	*	*

* After reset, these bits reflect the corresponding value of the mode input (that is, MODD, MODC, MODB, or MODA, respectively).

Reserved bit. Read as zero; write to zero for future compatibility

Figure 4-2. Operating Mode Register (OMR)

Area to Change	Change Description
Table 4-3, p. 4-17	• For bit 7, change the third line in Note 1 to the following: Instruction Cache always uses the highest internal Program RAM

4 Bus Control Register (BCR) Layout and Definition

Area to Change	Change Description
Figure 4-6, p. 4-25	• Replace with the following:

Change **Figure 4-6** of the *DSP56303 User's Manual* to the following figure:

23	22	21	20	19	18	17	16	15	14	13	12
BRH		BBS	BDFW4	BDFW3	BDFW2	BDFW1	BDFW0	BA3W2	BA3W1	BA3W0	BA2W2
11	**10**	**9**	**8**	**7**	**6**	**5**	**4**	**3**	**2**	**1**	**0**
BA2W1	BA2W0	BA1W4	BA1W3	BA1W2	BA1W1	BA1W0	BA0W4	BA0W3	BA0W2	BA0W1	BA0W0

Reserved bit. Read as zero; write to zero for future compatibility

Figure 4-6. Bus Control Register (BCR)

Area to Change	Change Description
Table 4-8, p. 4-26	• Change the row contents for bit 22 to the following:

22		0	Reserved. Write to 0 for future compatibility.

5 SCI Receive Register (SRX) Description

Area to Change	Change Description
Section 8.6.4.1, p. 8-23	• Change the beginning of the fourth paragraph from "In Synchronous mode" to "In Asynchronous mode".

6 Updated Programming Sheets

Use the following examples to replace **Figure B-2** (p. B-13), **Figure B-6** (p. B-17), and **Figure B-8** (p. B-19).

Application:_____ Date:_____

_____ Programmer:_____

Sheet 2 of 2

Central Processor

Bus Release Timing, Bit 12
0 = Fast Bus Release mode
1 = Slow Bus Release mode

Chip Operating Mode, Bits 3–0
Refer to the operating modes table in Chapter 4.

Asynchronous Bus Arbitration Enable, Bit 13
0 = Synchronization disabled
1 = Synchronization enabled

External Bus Disable, Bit 4
0 = Enables external bus
1 = Disables external bus

Address Attribute Priority Disable, Bit 14
0 = Priority mechanism enabled
1 = Priority mechanism disabled

Stop Delay Mode, Bit 6
0 = Delay is 128K clock cycles
1 = Delay is 16 clock cycles

Address Trace Enable, Bit 15
0 = Address Trace mode disabled
1 = Address Trace mode enabled

Memory Switch Mode, Bit 7
0 = Memory switching disabled
1 = Memory switching enabled

Stack Extension X Y Select, Bit 16
0 = Mapped to X memory
1 = Mapped to Y memory

Core-DMA Priority, Bits 9–8

CPD[1:0]	Description
00	Compare SR[CP] to active DMA channel priority
01	DMA has higher priority than core
10	DMA has same priority as core
11	DMA has lower priority than core

Stack Extension Underflow Flag, Bit 17
0 = No stack underflow
1 = Stack underflow

Stack Extension Overflow Flag, Bit 18
0 = No stack overflow
1 = Stack overflow

Cache Burst Mode Enable, Bit 10
0 = Burst Mode disabled
1 = Burst Mode enabled

Stack Extension Wrap Flag, Bit 19
0 = No stack extension wrap
1 = Stack extension wrap (sticky bit)

$\overline{TA}$ Synchronize Select, Bit 11
0 = Not synchronized
1 = Synchronized

Stack Extension Enable, Bit 20
0 = Stack extension disabled
1 = Stack extension enabled

23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
* 0	* 0	* 0	SEN	WRP	EOV	EUN	XYS	ATE	APD	ABE	BRT	TAS	BE	CPD1	CPD0	MS	SD	* 0	EBD	MD	MC	MB	MA

Operating Mode Register
Reset = $00030X; X = latched from levels on Mode pins

* = Reserved, Program as 0

Figure B-2. Operating Mode Register (OMR)

Application:_____ Date:_____

_____ Programmer:_____

Sheet 1 of 2

Bus Interface Unit

NOTE: All BCR bits are read/write control bits.

Bus Request Hold, Bit 23

0 = $\overline{BR}$ pin is asserted only for attempted or pending access

1 = $\overline{BR}$ pin is always asserted

Default Area Wait Control, Bits 20–16

Area 3 Wait Control, Bits 15–13

Area 2 Wait Control, Bits 12–10

Area 1 Wait Control, Bits 9–5

Area 0 Wait Control, Bits 4– 0

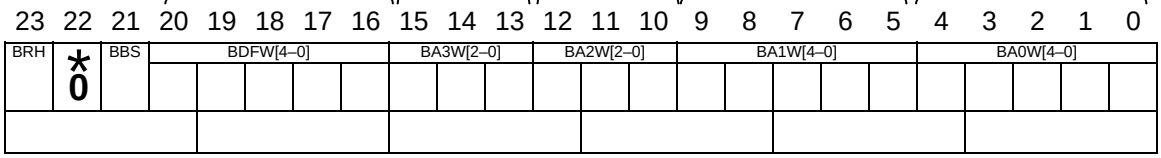
These read/write control bits define the number of wait states inserted into each external SRAM access to the designated area. The value of these bits should not be programmed as zero.

Bits	Bit Name	# of Wait States
20–16	BDFW[4–0]	0–31
15–13	BA3W[2–0]	0–7
12–10	BA2W[2–0]	0–7
9–5	BA1W[4–0]	0–31
4–0	BA0W[4–0]	0–31

Bus State, Bit 21

0 = DSP is not bus master

1 = DSP is bus master



Bus Control Register (BCR) **X:$FFFFFB Read/Write**

Reset = $1FFFFF

* = Reserved, Program as 0

Figure B-6. Bus Control Register (BCR)

Application:_____ Date:_____

_____ Programmer:_____

Sheet 3 of 3

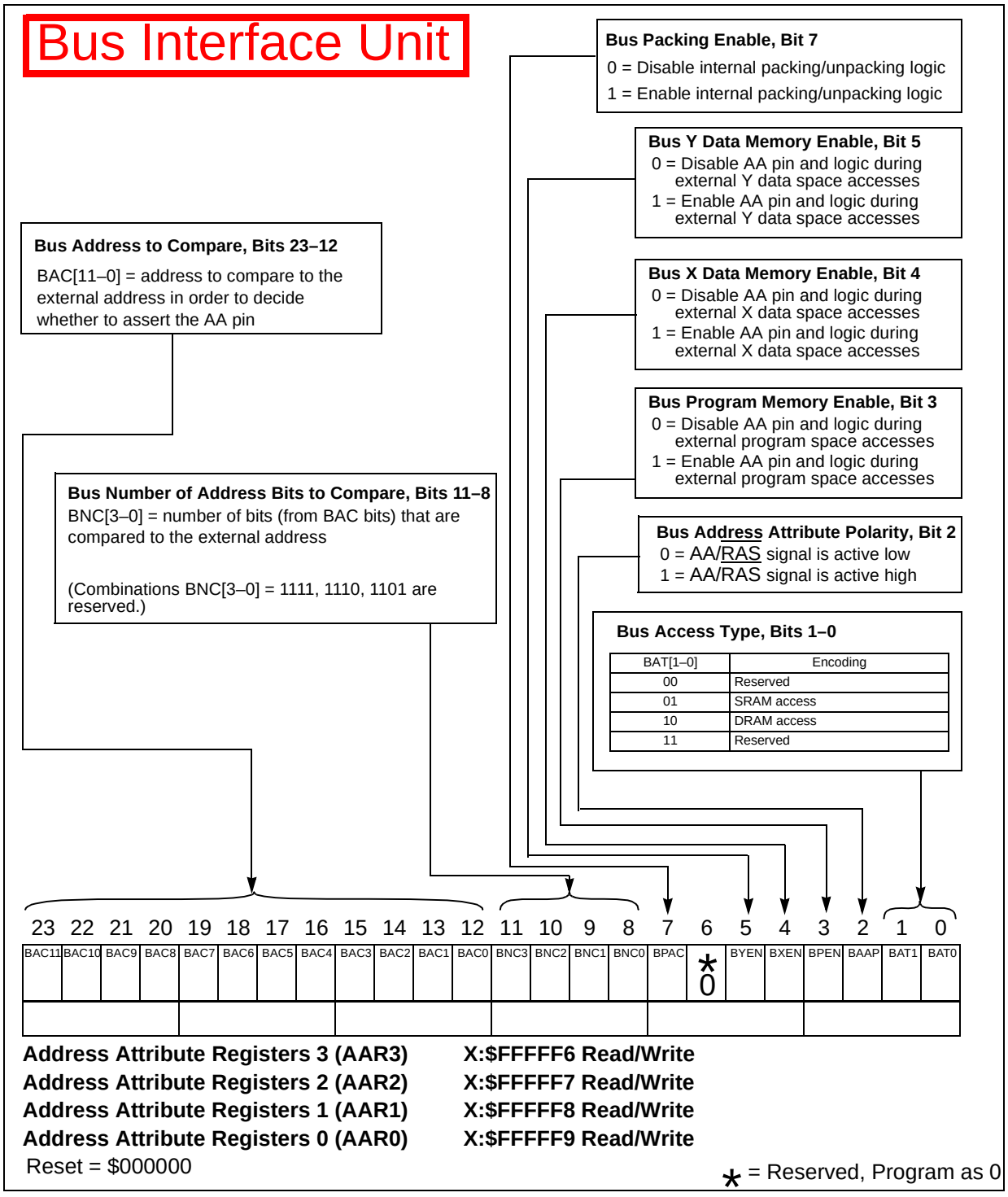


Figure B-8. Address Attribute Registers (AAR[3–0])

HOW TO REACH US:

USA/EUROPE/LOCATIONS NOT LISTED:

Motorola Literature Distribution;
P.O. Box 5405, Denver, Colorado 80217
1-303-675-2140 or 1-800-441-2447

JAPAN:

Motorola Japan Ltd.; SPS, Technical Information Center,
3-20-1, Minami-Azabu Minato-ku, Tokyo 106-8573 Japan
81-3-3440-3569

ASIA/PACIFIC:

Motorola Semiconductors H.K. Ltd.; Silicon Harbour Centre, 2 Dai King Street, Tai Po Industrial Estate,
Tai Po, N.T., Hong Kong
852-26668334

TECHNICAL INFORMATION CENTER:

1-800-521-6274

HOME PAGE:

http://www.motorola.com/semiconductors

DSP56303UMAD/D