Zynq MicroZed - SBC - B	
Avnet Engineering Services	
www.microzed.org	
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MicroZed - SBC - Rev B

5/7/2014

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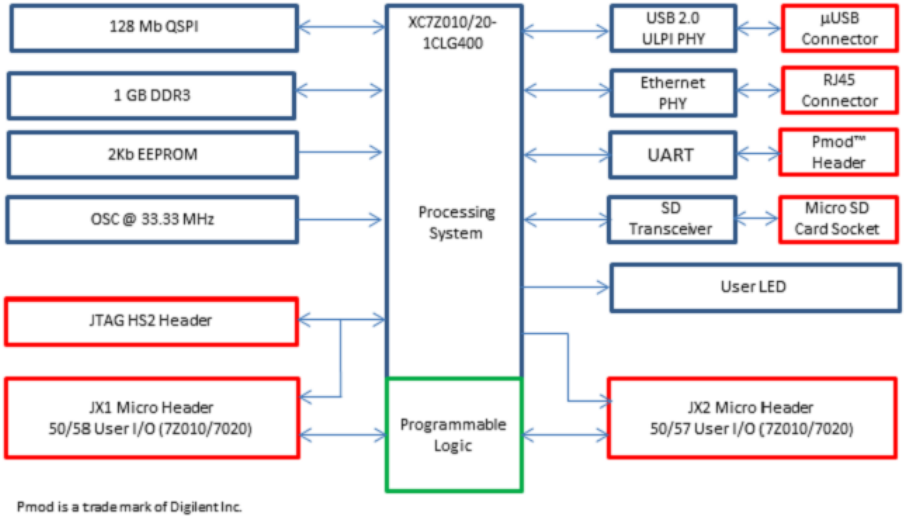
Avnet Engineering Services		
Title: 01 - Avnet Lead Sheet_B.SchDoc		
Size: B	Document Number: MicroZed - SBC	Rev: B
Date: 5/7/2014	Sheet 1 of 11	



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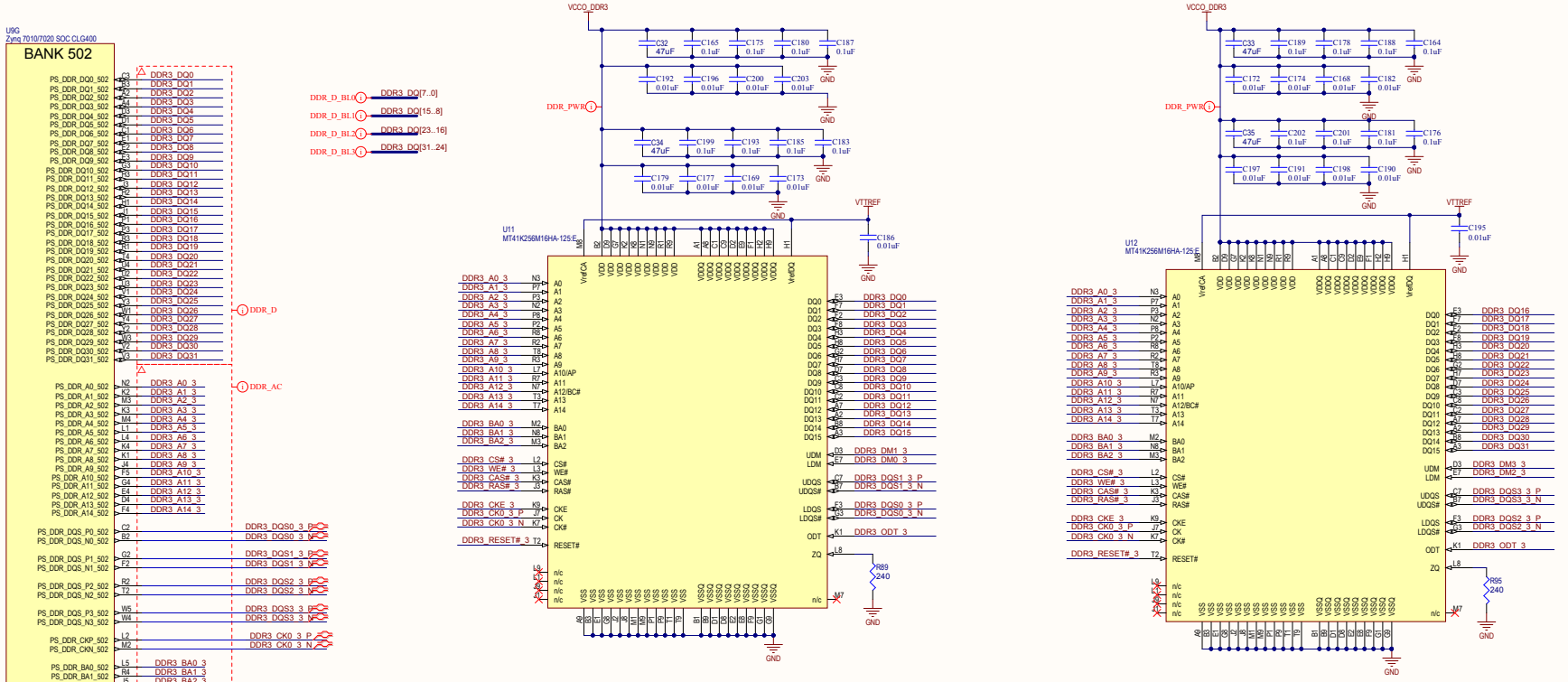
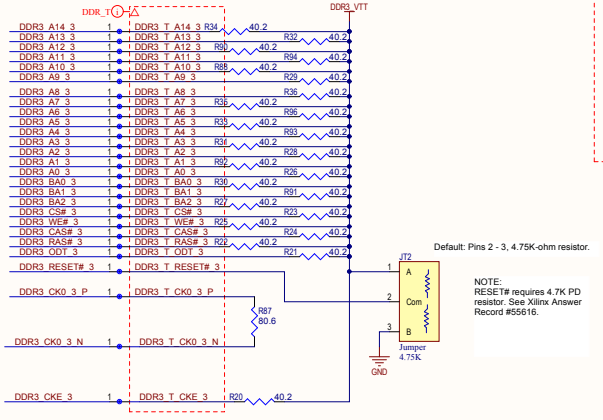
Size: B	Document Number: MicroZed - SBC	Rev: B
Date: 5/7/2014	Sheet 2 of 11	



Layout Note:
Use Fly-by routing and termination for DDR3 control signals.
Resistors should be placed past the last memory IC & as close to the device as possible.

Layout Note:
DDR3 trace lengths must include Zynq package flight times.
See UG933 and Layout Guidelines.

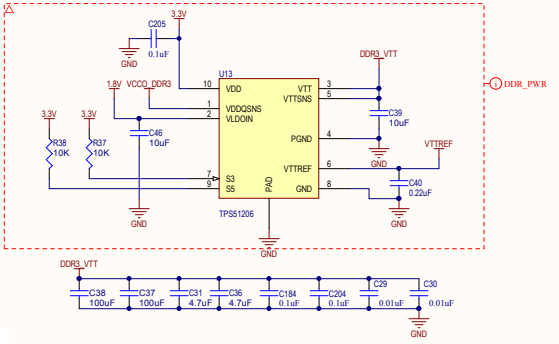
Layout Note:
DDR3 target trace impedances are as follows:
Single Ended Signals = 40 ohms
Differential Signals = 80 ohms



Default: Pins 2 - 3, 4.75K-ohm resistor.

NOTE:
RESET# requires 4.7K PD resistor. See Xilinx Answer Record #55616.

DDR3 Termination Supply



AVNET	Avnet Engineering Services
Title:	03 - DDR3.SchDoc
Size: C	Document Number: MicroZed - SBC
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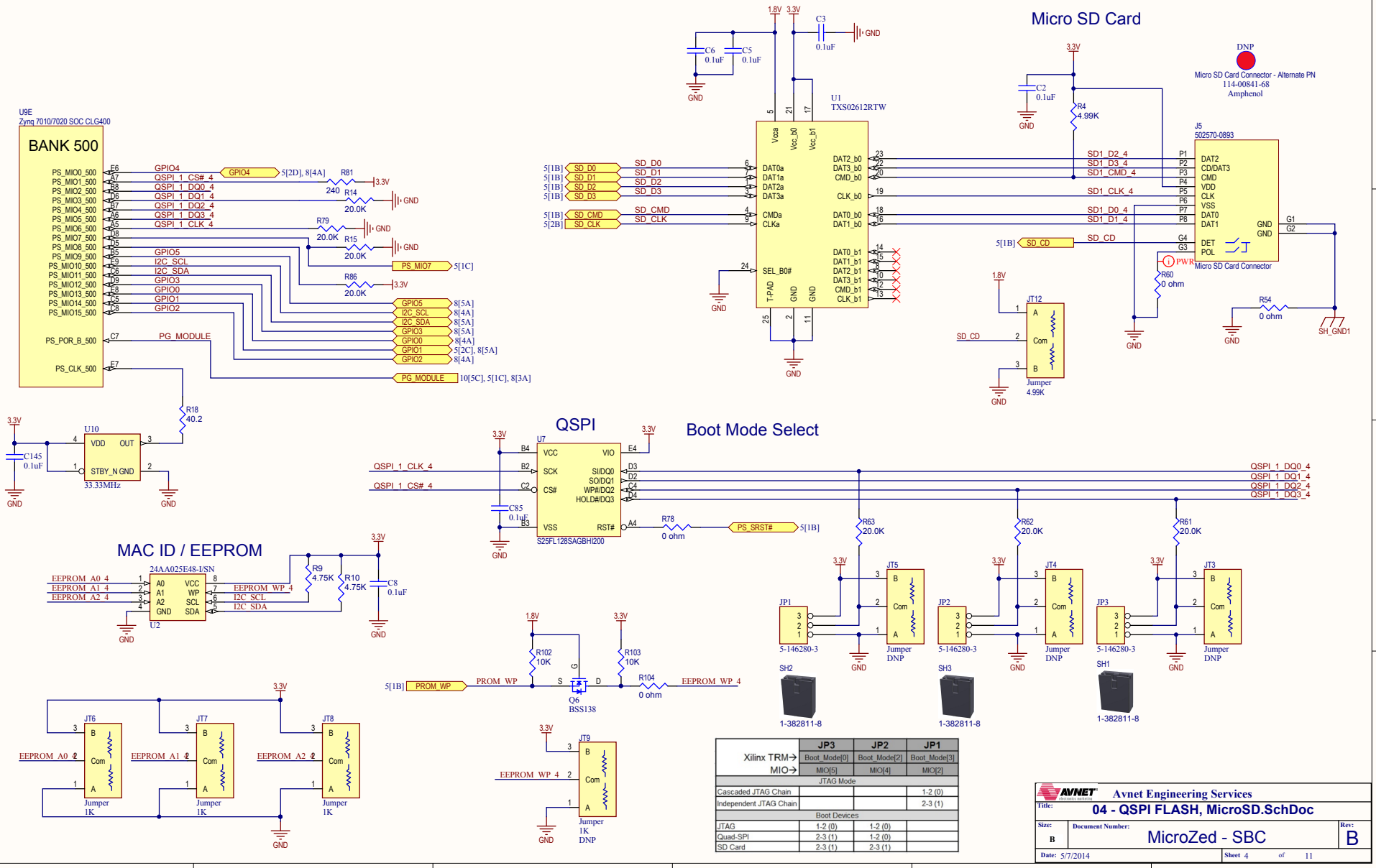

Xilinx TRM→	JP3	JP2	JP1
MIO→	Boot_Mode[0]	Boot_Mode[2]	Boot_Mode[3]
	MIO[5]	MIO[4]	MIO[2]
JTAG Mode			
Cascaded JTAG Chain			1-2 (0)
Independent JTAG Chain			2-3 (1)
Boot Devices			
JTAG	1-2 (0)	1-2 (0)	
Quad-SPI	2-3 (1)	1-2 (0)	
SD Card	2-3 (1)	2-3 (1)	

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Title: 04 - QSPI FLASH, MicroSD.SchDoc

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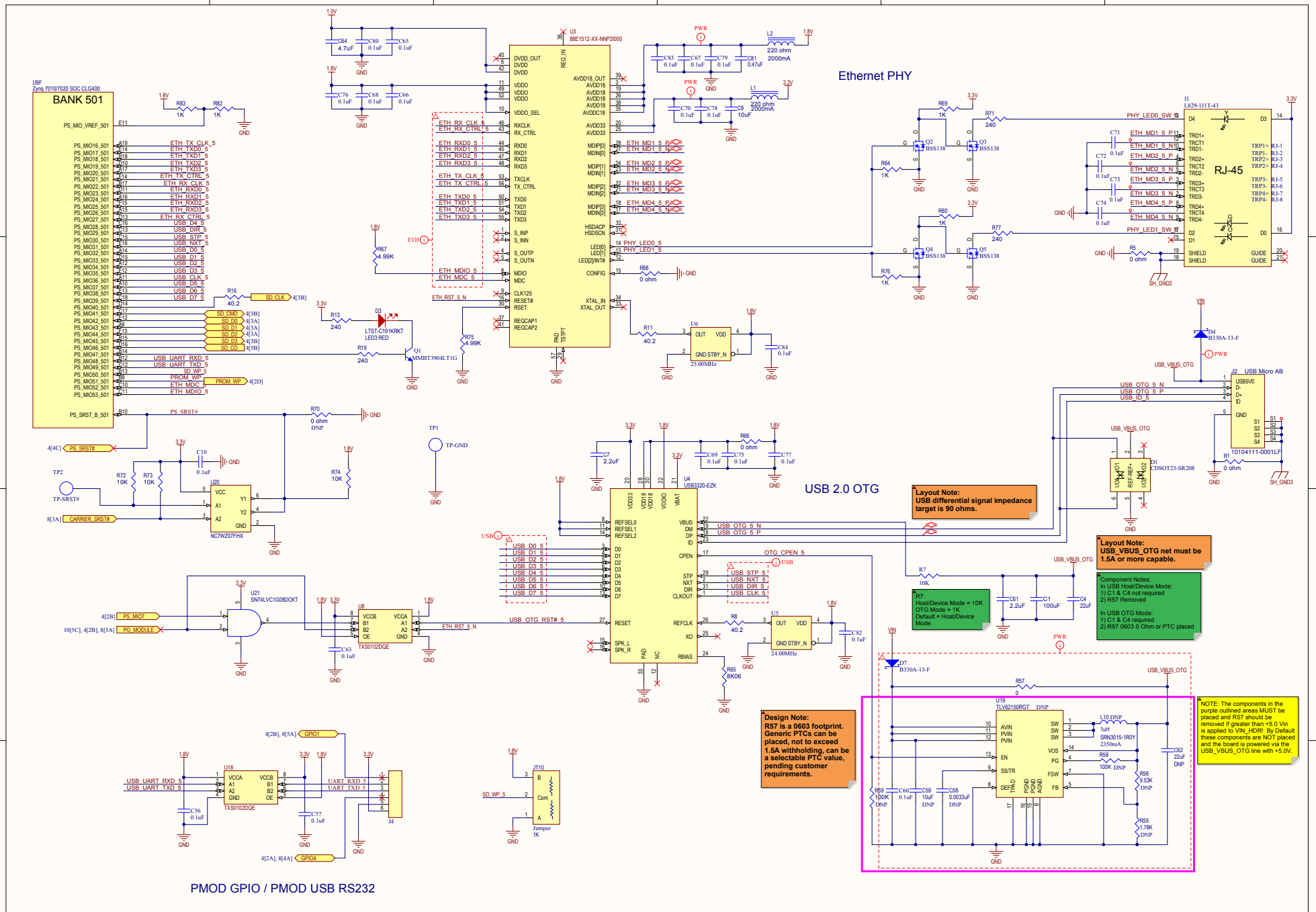
Ethernet PHY
USB 2.0 OTG
PMOD GPIO / PMOD USB RS232
BANK 501
RJ-45
USB Micro AB
Layout Note:
USB differential signal impedance target is 90 ohms.
Layout Note:
USB_VBUS_OTG net must be 1.5A or more capable.
Component Notes:
In USB Host/Device Mode:
1) C1 & C4 not required
2) R57 Removed
In USB OTG Mode:
1) C1 & C4 required
2) R57 0603 0 Ohm or PTC placed
R7:
Host/Device Mode = 10K
OTG Mode = 1K
Default = Host/Device Mode.
Design Note:
R57 is a 0603 footprint. Generic PTCs can be placed, not to exceed 1.5A withholding, can be a selectable PTC value, pending customer requirements.
NOTE: The components in the purple outlined areas MUST be placed and R57 should be removed if greater than +5.0 Vin is applied to VIN_HDR! By Default these components are NOT placed and the board is powered via the USB_VBUS_OTG line with +5.0V.
Avnet Engineering Services
Title: 05 - ETHERNET, USB.SchDoc
Size: C
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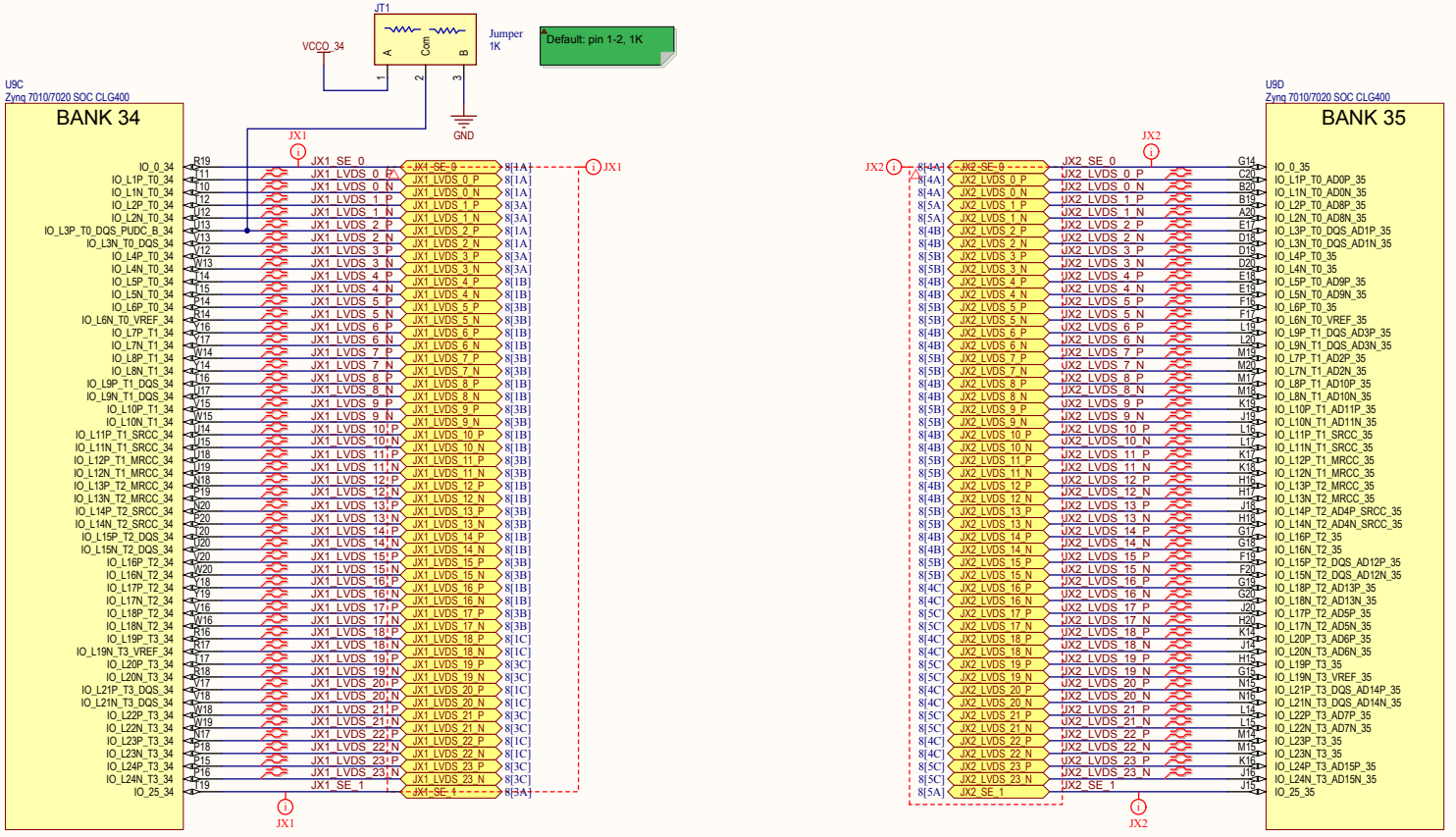

AVNET	Avnet Engineering Services		
Title:	06 - BANKS 34 and 35.SchDoc		
Size: B	Document Number: MicroZed - SBC		Rev: B
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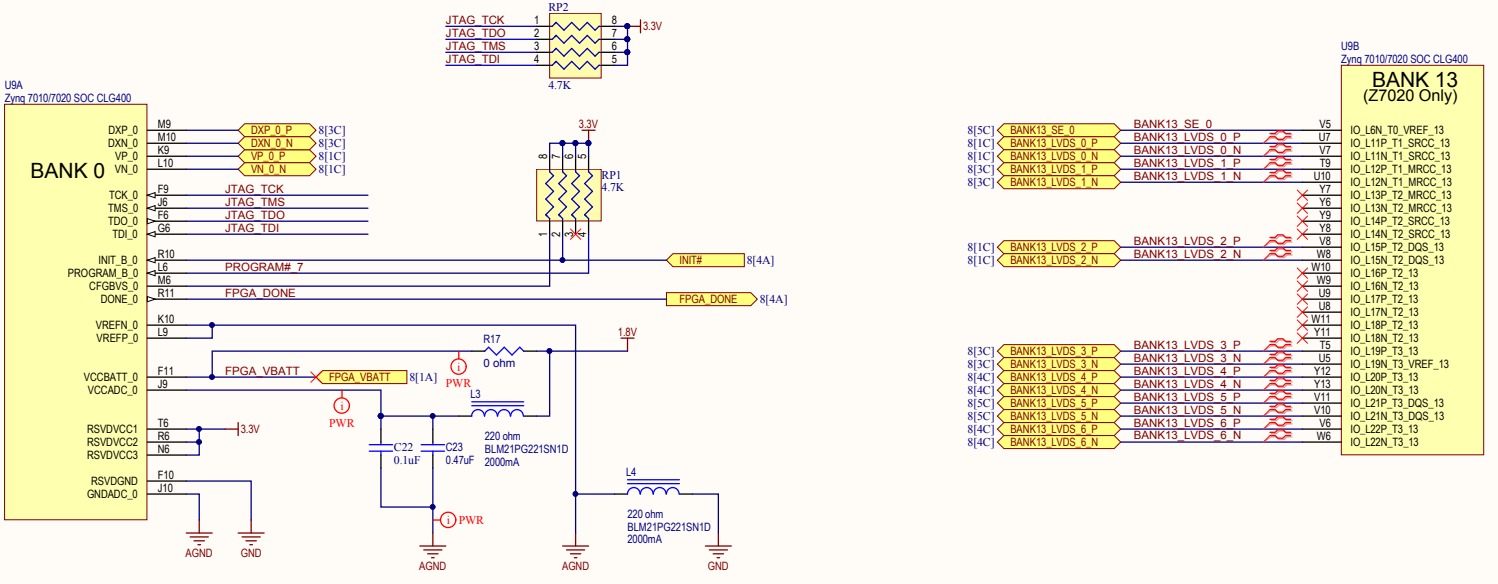

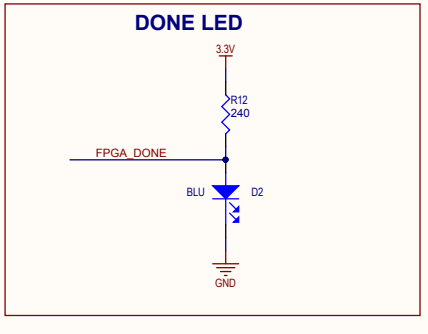

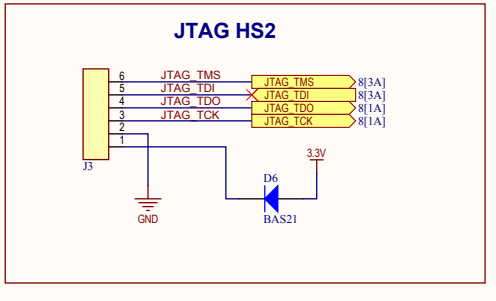

Avnet Engineering Services	
Title:	07 - BANK 0, BANK13, JTAG.SchDoc
Size: B	Document Number: MicroZed - SBC
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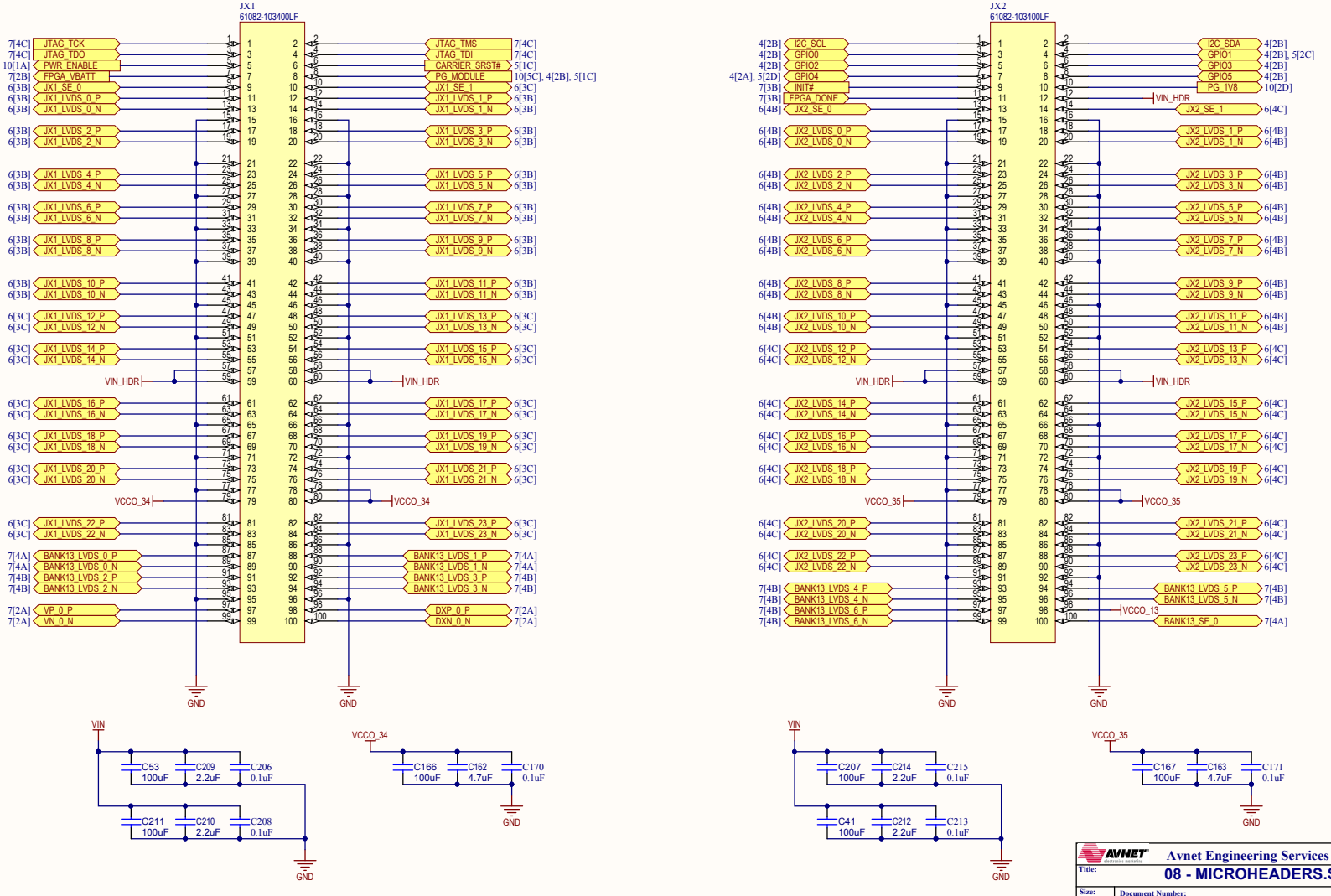

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Title:	08 - MICROHEADERS.SchDoc	
Size: B	Document Number: MicroZed - SBC	Rev: B
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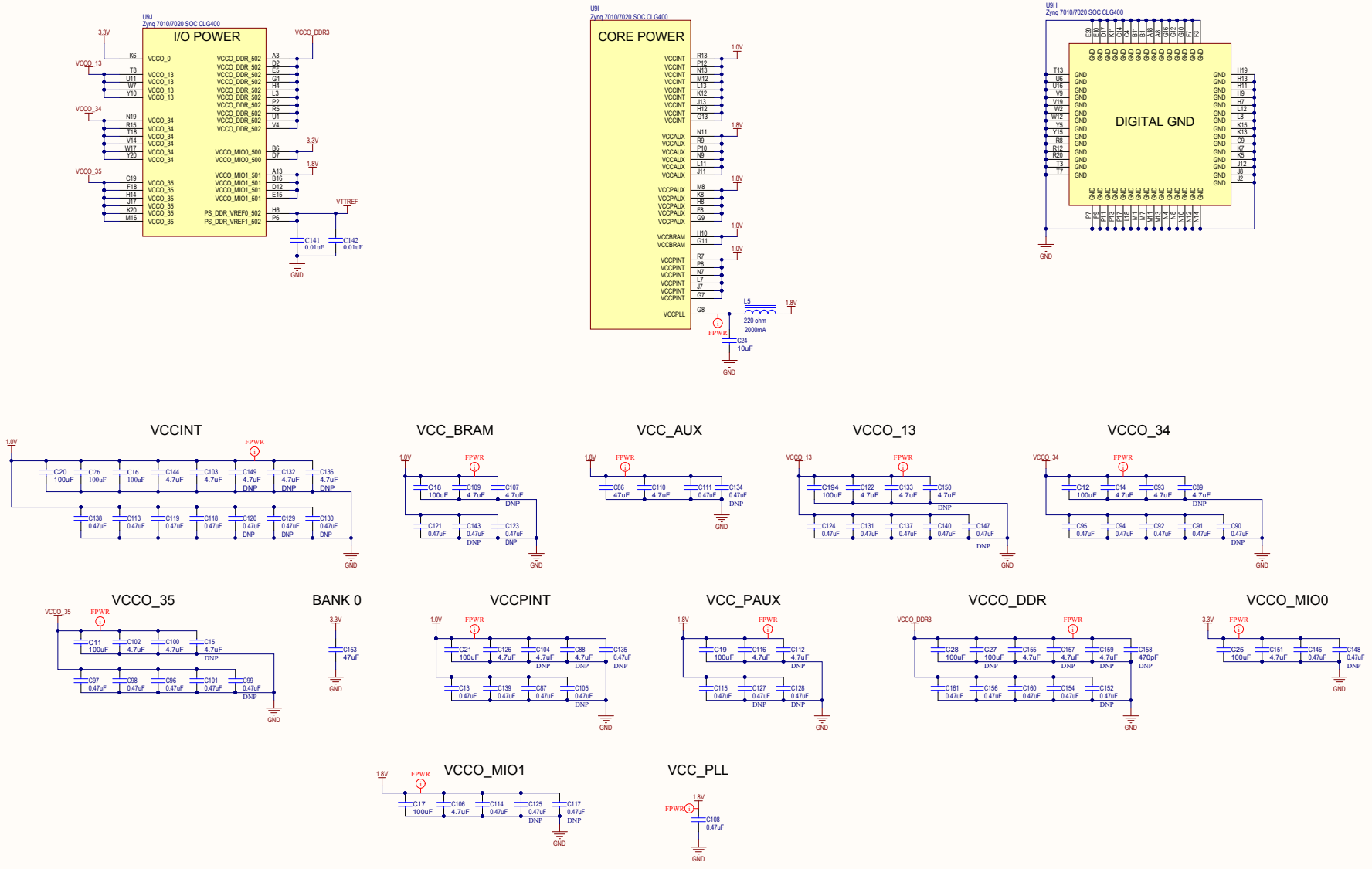

AVNET Avnet Engineering Services	
Title:	09 - FPGA POWER.SchDoc
Size: C	Document Number: MicroZed - SBC
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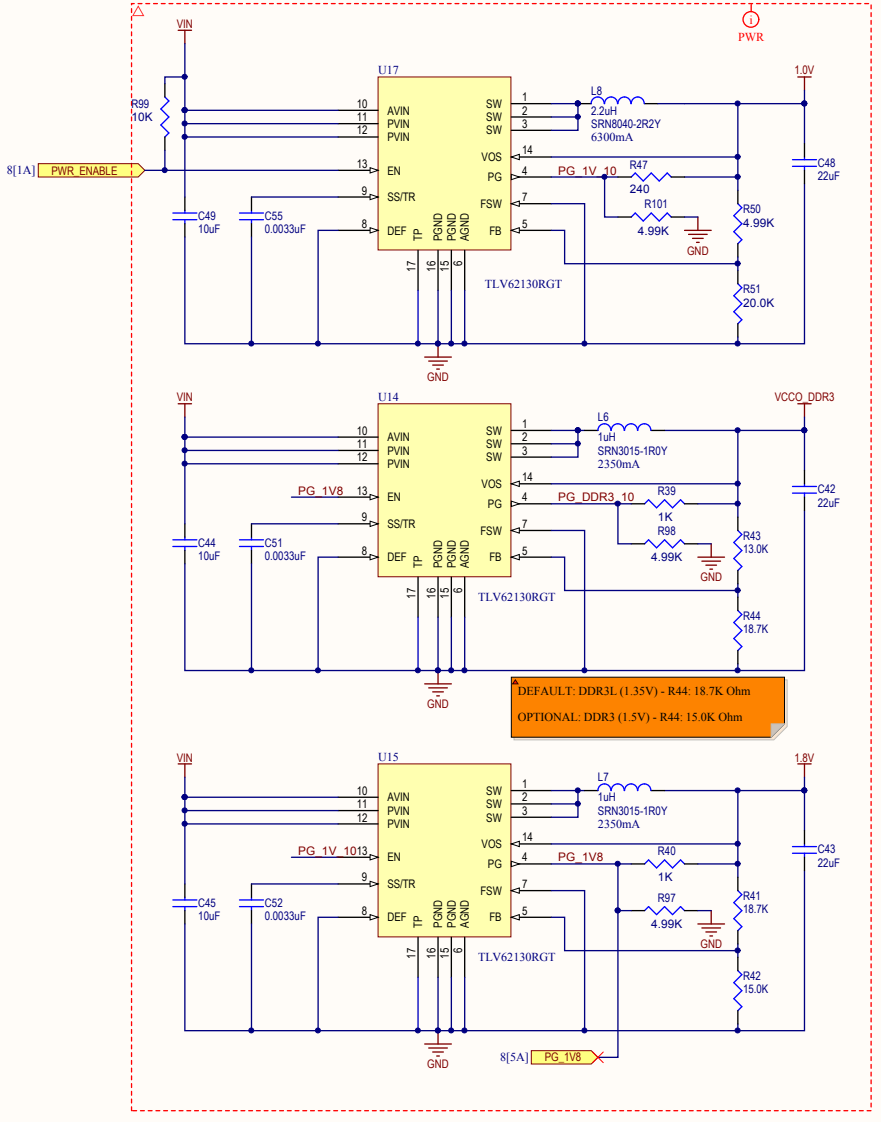
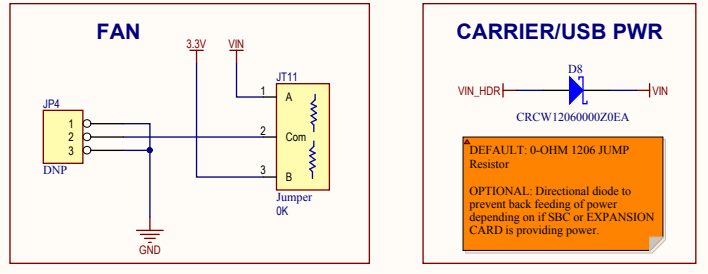
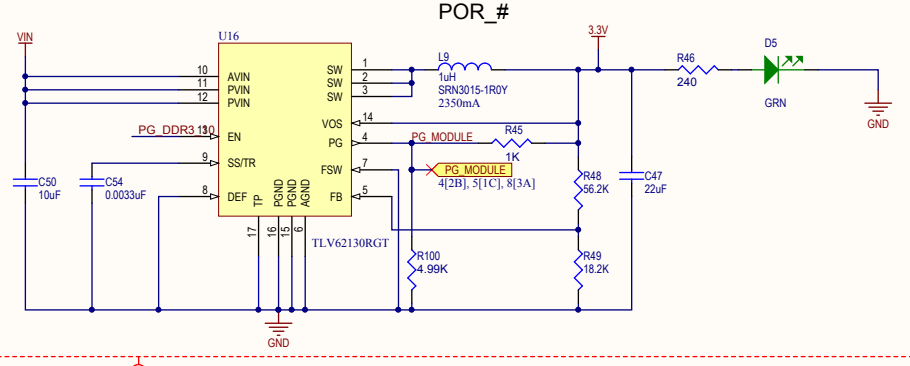
Date: 5/7/2014	Sheet 9 of 11







AVNET Engineering Services	Avnet Engineering Services
Title:	10 - POWER, RESET.SchDoc
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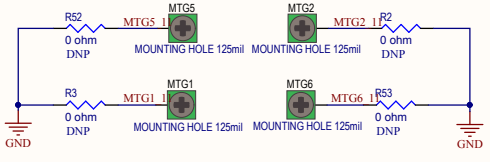
Revision Notes:

Revision SBC Changes:
1) Page 2: Updated Block Diagram
2) Page 3: DDR3_RESET Resistor per Xilinx Answer Record #55616
3) Page 3: DDR3 Voltage Rails Renamed
4) Page 4: EEPROM WP Translator
5) Page 4: SD Card Dual Footprint Connector
6) Page 4: SD Card Detect PD/PU Resistor
7) Page 5: EEPROM WP Control from PS
8) Page 5: USB VBUS Resistor Default Switched from 1K to 10K
9) Page 9: DDR Voltage Rails Renamed
10) Page 10: PG_1V Voltage Divider Resitor R47 Updated
11) Page 10: DDR3 Voltage Rail Renamed
12) Page 11: DDR3 Voltage Rail 1.35V / 1.5V Option Provided

Mechanicals:

PCB
Z7MB-Z70x0-PCB-SBC-A

PCB Mounting Holes



Fansink Mounting Holes

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Title: 11 - Back Page.SchDoc		
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